

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	917	703/1.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/03/06 09:57

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	1352	eda and network and @ad<"20030330"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/03/06 12:10
L4	615	L3 and design adj automation	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/03/06 12:11
L5	2	("6157947"   "6507944").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/03/06 13:03
L6	1	"20040078670".pn.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/03/06 13:19
L7	1	"5878053".pn.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/03/06 13:19
L8	8	("20020002524"   "20020019836"   "5418954"   "5794210"   "5855008"   "5933498"   "6006332"   "6157947").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/03/06 13:44
L9	2	"6687710".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/03/06 13:44
L10	8	("20020002524"   "20020019836"   "5418954"   "5794210"   "5855008"   "5933498"   "6006332"   "6157947").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/03/06 13:44
L11	7	("5862223"   "5878408"   "5933356"   "6058426"   "6102961"   "6141724"   "6269467").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/03/06 13:46

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- ☐ **1. An Industrial view of electronic design automation**  
MacMillen, D.; Camposano, R.; Hill, D.; Williams, T.W.;  
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on  
Volume 19, Issue 12, Dec. 2000 Page(s):1428 - 1448  
Digital Object Identifier 10.1109/43.898825  
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(180 KB\)](#) IEEE JNL  
[Rights and Permissions](#)
- ☐ **2. EDA in IBM: past, present, and future**  
Darringer, J.; Davidson, E.; Hathaway, D.J.; Koenemann, B.; Lavin, M.; Morrell, J.K.; Rahmat, K.; Roesner, W.;  
Schanzenbach, E.; Tellez, G.; Trevillyan, L.;  
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on  
Volume 19, Issue 12, Dec. 2000 Page(s):1476 - 1497  
Digital Object Identifier 10.1109/43.898827  
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(320 KB\)](#) IEEE JNL  
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- ☐ **3. Subject Index**  
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on  
Volume 19, Issue 12, Dec. 2000 Page(s):5 - 19  
Digital Object Identifier 10.1109/TCAD.2000.898836  
[AbstractPlus](#) | Full Text: [PDF\(128 KB\)](#) IEEE JNL  
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- ☐ **4. IEEE standard for Integrated circuit (IC) delay and power calculation system**  
26 June 1999 Page(s):i - 390  
[AbstractPlus](#) | Full Text: [PDF\(1780 KB\)](#) IEEE STD
- ☐ **5. WELD-an environment for Web-based electronic design**  
Chan, F.L.; Spiller, M.D.; Newton, A.R.;  
Design Automation Conference, 1998. Proceedings  
15-19 Jun 1998 Page(s):146 - 151  
[AbstractPlus](#) | Full Text: [PDF\(576 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ **6. Electronic CAD frameworks**  
Harrison, D.S.; Newton, A.R.; Spickelmier, R.L.; Barnes, T.J.;  
Proceedings of the IEEE  
Volume 78, Issue 2, Feb. 1990 Page(s):393 - 417  
Digital Object Identifier 10.1109/5.52218  
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- ☐ 1. EDA-GARDS Universal Gate Array Design System  
[Computer Graphics and Applications, IEEE](#)  
Volume 2, Issue 4, Jun 1982 Page(s):15 - 15  
[AbstractPlus](#) | Full Text: [PDF\(944 KB\)](#) IEEE JNL  
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- ☐ 2. European activities for EDA standardization  
Sauer, A.; Tual, J.P.; La Fontaine, R.;  
[Micro, IEEE](#)  
Volume 12, Issue 4, Aug. 1992 Page(s):54 - 59  
Digital Object Identifier 10.1109/40.149736  
[AbstractPlus](#) | Full Text: [PDF\(512 KB\)](#) IEEE JNL  
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- ☐ 3. The EDA business model dialogue part 1  
Prabhu, A.;  
[Design & Test of Computers, IEEE](#)  
Volume 12, Issue 3, Autumn/Fall 1995 Page(s):6  
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[AbstractPlus](#) | [References](#) | Full Text: [PDF\(368 KB\)](#) IEEE JNL  
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- ☐ 4. Managing your EDA Investments  
Prabhu, A.;  
[Design & Test of Computers, IEEE](#)  
Volume 12, Issue 1, Spring 1995 Page(s):5 - 7, 89-90  
Digital Object Identifier 10.1109/54.350669  
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(392 KB\)](#) IEEE JNL  
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- ☐ 5. The EDA Business Model Dialogue Part 2  
Prabhu, A.;  
[Design & Test of Computers, IEEE](#)  
Volume 12, Issue 4, Winter 1995 Page(s):4  
Digital Object Identifier 10.1109/MDT.1995.473306  
[AbstractPlus](#) | Full Text: [PDF\(296 KB\)](#) IEEE JNL  
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- ☐ 6. Facets of growth in the EDA market  
Prabhu, A.;  
[Design & Test of Computers, IEEE](#)  
Volume 13, Issue 2, Summer 1996 Page(s):5 - 6  
Digital Object Identifier 10.1109/54.500193

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**Electronic design automation tool for the design of a semiconductor integrated circuit chip - group of 3 »**

RS Tsay, CC Chang - US Patent 5,461,576, 1995 - Google Patents

... US005461576A [li] Patent Number: [45] Date of Patent: [54] **ELECTRONIC DESIGN AUTOMATION TOOL FOR THE DESIGN OF A SEMICONDUCTOR INTEGRATED CIRCUIT CHIP ...**

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**Prime: a timing-driven placement tool using a piecewise linear resistive network approach - group of 2 »**

T Hamada, CK Cheng, PM Chau - Proceedings of the 30th international on Design automation ..., 1993 - portal.acm.org

... driven placement tool using a piecewise linear resistive **network** approach. ... Sponsors, EDAC : **Electronic Design Automation** Consortium IEEE-CAS : Circuits & Systems ...

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**Electronic design automation apparatus and method utilizing a physical information database - group of 2 »**

J Loos, CY Wang, M Mahmood... - US Patent 5,487,018, 1996 - Google Patents

... The development of ASICs with CAD tools is often referred to as **Electronic Design Automation** (EDA). 15 ... A datapath design is a **network** of 45 ...

[Cited by 34](#) - [Related Articles](#) - [Web Search](#)

**[book] Introduction to VLSI Systems - group of 2 »**

C Mead, L Conway - 1979 - Addison-Wesley Longman Publishing Co., Inc. Boston, MA, USA

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**Test generation for large logic networks**

PS Bottorff, RE France, NH Garges, EJ Orosz - Proceedings of the 14th conference on Design automation, 1977 - portal.acm.org

... The **network** to be tested is assumed to comply with a set of ground rules for testability. The system includes features for automatic ...

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**A parallel bottom-up clustering algorithm with applications to circuit partitioning in VLSI design - group of 2 »**

J Cong - Proceedings of the 30th international conference on Design ..., 1993 - portal.acm.org

... Sponsors, EDAC : **Electronic Design Automation** Consortium IEEE-CAS : Circuits & Systems ... A linear-time heuristic for improving **network** partitions, Proceedings of ...

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**Work group computing for electronic design automation - group of 2 »**

FB Heile, BA Fairbanks - US Patent 5,983,277, 1999 - Google Patents

... 900 -908 Mass Storage **Network** Connection 972- CD-ROM Processors) ... 904 Primary Storage Page 18. 5,983,277 WORK GROUP COMPUTING FOR **ELECTRONIC DESIGN AUTOMATION** ...

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**Performance-driven Steiner tree algorithm for global routing - group of 3 »**

X Hong, T Xue, ES Kuh, CK Cheng, J Huang - Proceedings of the 30th international conference on Design ..., 1993 - portal.acm.org

... Sponsors, EDAC : **Electronic Design Automation** Consortium IEEE-CAS : Circuits & Systems SIGDA: ACM ... Xu , HaiYun Bao , Jun Gu, CNB: a critical-**network**-based timing ...

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**Applications of pixel detectors to electron microscopy • ARTICLE**  
*Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Volume 512, Issues 1-2, 11 October 2003, Pages 310-317*  
A. R. Faruqi, D. M. Cattermole and C. Raeburn  
[Abstract](#) | [Abstract + References](#) | [PDF \(292 K\)](#)

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-  2. ☐


**Dynamic energy-consumption indicators for domestic appliances: environment, behaviour and design • ARTICLE**  
*Energy and Buildings, Volume 35, Issue 8, September 2003, Pages 821-841*  
G. Wood and M. Newborough  
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**Rapid prototyping for wireless designs: the five-ones approach • ARTICLE**  
*Signal Processing, Volume 83, Issue 7, July 2003, Pages 1427-1444*  
Markus Rupp, Andreas Burg and Eric Beck  
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-  4. ☐


**AWR, TriQuint, & Multilink Collaborate to Streamline MMIC Design & Development • ARTICLE**  
*III-Vs Review, Volume 15, Issue 7, September 2002, Pages 36-40*  
Ted Miracco and Mark A. Saffian  
[Abstract](#) | [Abstract + References](#) | [PDF \(646 K\)](#)

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**Handling advanced scheduling heuristics under a hardware compiler generation environment • ARTICLE**  
*Knowledge-Based Systems, Volume 15, Issues 1-2, January 2002, Pages 3-11*  
George Economakos, Petros Oikonomakos, Ioannis Poulakis, George Papakonstantinou and Stamatis Georgoulis  
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**A system for evaluating sheet formability using tensile tests with different shapes of specimens • ARTICLE**  
*Journal of Materials Processing Technology, Volume 116, Issues 2-3, 24 October 2001, Pages 189-193*

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**Intellectual property re-use in embedded system co-design: an industrial case study - group of 8 »**

E Filippi, L Lavagno, L Licciardi, A Montanaro, M ... - System Synthesis, 1998. Proceedings. 11th International ..., 1998 - [ieeexplore.ieee.org](#)

... an industrial telecom system design, an ATM node **server**. ... while the use of customizable IP modules leads ... experience in designing an industrial **test** case using ...

Cited by 16 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**ETA: Experience with a Intel R Xeon TM Processor as a Packet Processing Engine - group of 12 »**

G Regnier, D Minturn, G McAlpine, V Saleto, A ... - Proc. of the Symposium on High Performance Interconnects - [doi.ieeeecomputersociety.org](#)

... of the interface between the **test** application and ... purpose Intel® Xeon TM Processor for **server**-based packet ... Buonadonna, D. Culler, "Queue-Pair IP: A Hybrid ...

Cited by 32 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**Mobile agents and intellectual property protection - group of 12 »**

SG Belmon, BS Yee - Personal Technologies, 1998 - Springer

... wants customers to be able to **test** new theories ... simple, natural, and elegant solutions for IP protection ... Once within the **server**, there are no access restrictions ...

Cited by 14 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**IP repository, a Web based IP reuse infrastructure**

P Schindler, K Weidenbacher, T Zimmermann - Custom Integrated Circuits, 1999. Proceedings of the IEEE ..., 1999 - [ieeexplore.ieee.org](#)

... compo- nents, also often described as **Intellectual Property** (tP ... to the central IP meta data **server**), should be ... eg digital, analog or software IP (**test** pro- grams ...

Cited by 13 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**The use of SystemC for design verification and integration test of IP-cores - group of 6 »**

A Fin, F Fummi, D Signoretto - ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE ..., 2001 - [ieeexplore.ieee.org](#)

... as soon the outputs are received from the core vendor **server** and it ... The proposed methodology for the verification and integra- tion **test** of IP cores is ...

Cited by 6 - [Related Articles](#) - [Web Search](#)

**Method, apparatus, system, and program storage device for distributing intellectual property - group of 3 »**

Y Watanabe, S Iino, Y Morita, K Nishimori, I ... - US Patent 6,157,947, 2000 - Google Patents

... users to receive information about the **intellectual property** on time and to optimally share the **intellectual property**. ... **SERVER** FOR DIVISION A REGISTER IP 250 ...

Cited by 11 - [Related Articles](#) - [Web Search](#)

**[book] Intellectual Property Protection in VLSI Design: Theory and Practice**

G Qu, M Potkonjak - 2003 - [books.google.com](#)

... 31.2 **Intellectual property** reuse-based design flow ... between Cases E and F may be high because of potential reused IP between these ... A thousand **test** cases were used ...

Cited by 6 - [Related Articles](#) - [Web Search](#) - [Library Search](#)

**Component Selection and Matching for IP-Based Design - group of 15 »**

T Zhang, L Benini, G De Micheli - ... Conference on Design, automation and **test** in Europe, Munich ..., 2001 - [doi.ieeeecomputersociety.org](#)

... fuzzy matching in Match Engine is run at the **server** side ... Proceedings of Design,

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**[A Structured Test Re-Use Methodology for Core-Based System Chips - group of 5 »](#)**

P Varma, S Bhatia - Proceedings IEEE International Test Conference (ITC), 1998 - doi.ieeecs.org

... In addition, previous **test** bus approaches do not satisfactorily ... the prob- lem of supporting IP with bi ... In this paper, a structured **automated test** bus methodology ...

Cited by 159 - [Related Articles](#) - [Web Search](#)

**[Automated Method to Generate Bitstream Intellectual Property Cores for Virtex FPGAs - group of 4 »](#)**

EL Horta, JW Lockwood - Proceedings of the 14 thField-Programmable Logic and ..., 2004 - Springer

**Automated** Method to Generate Bitstream ... a partial bitstream from full bitstream files, enables the chip developer to generate, develop and **test** an IP core in ...

Cited by 9 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**[Essential Issues for IP Reuse - group of 4 »](#)**

DD Gajski, ACH Wu, V Chaikyakul, S Mori, T Nukiyama ... - Proc. ASP-DAC, 2000 - doi.ieeecomputersociety.org

... user manuals, simulation and reuse models, **test** benches and ... and evaluation, is another issue for IP providers. ... in this area, information for **automated** or semi ...

Cited by 24 - [Related Articles](#) - [Web Search](#)

**[On the Test of Microprocessor IP Cores - group of 17 »](#)**

F Corno, MS Reorda, G Squillero, M Violante - IEEE Design, Automation & Test in Europe, 2001 - doi.ieeecomputersociety.org

... The method can be partially **automated**, and combines ... by the availability of **Intellectual Property (IP)** cores provided ... **Testing** SOC's is rapidly becoming a major ...

Cited by 39 - [Related Articles](#) - [Web Search](#)

**[Component Selection and Matching for IP-Based Design - group of 15 »](#)**

T Zhang, L Benini, G De Micheli - Proceedings, Conference on Design, automation and test in ..., 2001 - doi.ieeecomputersociety.org

... Second, we propose an **automated IP** component selection technique based ... IP query and specification are parsed to the ... of Design, Automation, and **Test** in Europe ...

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**[Intellectual property re-use in embedded system co-design: an industrial case study - group of 8 »](#)**

E Filippi, L Lavagno, L Licciardi, A Montanaro, M ... - System Synthesis, 1998. Proceedings. 11th International ..., 1998 - ieeexplore.ieee.org

... VIP Library™ is a library of customizable IP soft cores ... onto gate level netlists through **automatic** synthesis ... phases but also in system integration and **testing**. ...

Cited by 16 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

**[A qualification platform for design reuse - group of 8 »](#)**

R Seepold, NM Madrid, A Vorg, W Rosenstiel, M ... - Quality Electronic Design, 2002. Proceedings. International ..., 2002 - ieeexplore.ieee.org

... This task has been **automated**. ... stalled and embedded into an existing design flow of an IP provider ... The **test** module consists of 13 megabytes of data in 260 files ...

Cited by 15 - [Related Articles](#) - [Web Search](#)

**[Timing abstraction of intellectual property blocks](#)**

SV Venkatesh, R Palermo, M Mortazavi, KA Sakallah, ... - Custom Integrated Circuits Conference, 1997., Proceedings of ..., 1997 - ieeexplore.ieee.org

... describe a novel approach for the **automatic** generation of ... repeated n + 1 times for